Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor integrated circuit device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns,

wherein each of the nonvolatile semiconductor memory devices comprises:

a word gate formed on a semiconductor layer with a first gate insulating layer ~~interposed~~therebetween;

an impurity diffusion layer which forms either a source region or a drain region; and

first and second control gates in the shape of sidewalls formed along either side of the word gate, wherein:

the first control gate is disposed on the semiconductor layer with a second gate insulating layer therebetween~~interposed~~, and also on the word gate with a side insulating layer therebetween~~interposed~~;

the second control gate is disposed on the semiconductor layer with another second gate insulating layer therebetween~~interposed~~, and also on the word gate with another side insulating layer therebetween~~interposed~~;

the first and second control gates extend in a first direction; and

a pair of the first and second control gates, adjacent each other in a second direction which intersects the first direction, are connected to each other through a pad-shaped common contact section, the pair of first and second control gates also being connected to an upper interconnect layer through a conductive layer disposed in a contact hole and formed over th pad-shaped common contact section.

2. (Original) The semiconductor integrated circuit device as defined in claim 1, wherein each of the first and second control gates is formed of a conductive layer extending in the direction in which the impurity diffusion layer extends.

3. (Previously Presented) The semiconductor integrated circuit device as defined in claim 1, wherein the common contact section is connected to the first and second control gates and includes a common contact section conductive layer formed of the same material as the first and second control gates.

4. (Previously Presented) The semiconductor integrated circuit device as defined in claim 1, wherein the common contact section includes an insulating layer formed on the semiconductor layer, a common contact section conductive layer formed on the insulating layer, and a cap layer formed on the common contact section conductive layer.

5. (Original) The semiconductor integrated circuit device as defined in claim 4, wherein the insulating layer is formed of a laminate consisting of a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.

6. (Original) The semiconductor integrated circuit device as defined in claim 1, wherein:

the side insulating layers are located between the word gate and the first and second control gates; and

the upper ends of the side insulating layers are located higher than the first and second control gates with respect to the semiconductor layer.

7. (Previously Presented) The semiconductor integrated circuit device as defined in claim 1, wherein:

a buried insulating layer is formed between the two side insulating layers disposed in contact with the first and second control gates; and

the buried insulating layer covers the adjacent first and second control gates.

8. (Original) The semiconductor integrated circuit device as defined in claim 1, wherein the common contact section is provided in contact with one end of the impurity diffusion layer.

9. (Original) The semiconductor integrated circuit device as defined in claim 1, wherein the common contact sections are staggered relative to each other.

10. (Original) The semiconductor integrated circuit device as defined in claim 1, wherein:

the memory cell array is divided into a plurality of blocks; and

the impurity diffusion layers in blocks adjacent to each other in the first direction are connected to each other through a contact impurity diffusion layer formed in the semiconductor layer.

11. (Original) The semiconductor integrated circuit device as defined in claim 1, wherein the second gate insulating layer is formed of a laminate consisting of a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.

12. (Original) The semiconductor integrated circuit device as defined in claim 1, wherein the side insulating layer is formed of a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.

13. (Previously Presented) A semiconductor integrated circuit device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns,

each of the nonvolatile semiconductor memory devices comprising:

a word gate formed on a semiconductor layer with a first gate insulating layer therebetween;

an impurity diffusion layer which forms either a source region or a drain region;

a first control gate formed along a first side of the word gate, the first control gate being disposed on the semiconductor layer with a second gate insulating layer therebetween, and also on the word gate with a side insulating layer therebetween;

a second control gate formed along a second side of the word gate, the second control gate being disposed on the semiconductor layer with another second gate insulating layer therebetween, and also on the word gate with another side insulating layer therebetween;

the first and second control gates extend in a first direction; and

an end of the first control gate and an end of the second control gate that are adjacent to each other in a second direction which intersects the first direction, are connected to each other through a pad-shaped common contact section, the end of the first control gate and the end of the second control gate also being connected to an upper interconnect layer through a conductive layer disposed in a contact hole and formed over the pad-shaped common contact section.

14. (Previously Presented) The semiconductor integrated circuit device of claim 13, wherein the first and second control gates are formed in the shape of sidewalls along either side of the word gate.

15. (Previously Presented) The semiconductor integrated circuit device of claim 13, wherein the common contact section includes an insulating layer formed on the semiconductor layer, the insulating layer formed of a laminate comprising a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.

16. (Previously Presented) The semiconductor int grated circuit device of claim 13, wherein the common contact sections are staggered relative to each other.

17. (Previously Presented) A semiconductor integrated circuit device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns,

wherein each of the nonvolatile semiconductor memory devices comprises:

a word gate formed on a semiconductor layer with a first gate insulating layer therebetween;

an impurity diffusion layer that forms either a source region or a drain region; and

first and second control gates formed along either side of the word gate in the shape of sidewalls, wherein:

the first control gate being disposed on the semiconductor layer with a second gate insulating layer therebetween, and also on the word gate with a side insulating layer therebetween;

the second control gate being disposed on the semiconductor layer with another second gate insulating layer therebetween, and also on the word gate with another side insulating layer therebetween;

the first and second control gates extend in a first direction; and

an end of the first control gate and an end of the second control gate of a pair of gates adjacent to each other in a second direction which intersects the first direction, are connected to each other through a pad-shaped common contact section that is disposed in a staggered arrangement relative an adjacent common contact section, the end of the first control gate and the end of the second control gate also being connected to an upper

interconnect layer through a conductive layer disposed in a contact hole and formed over the pad-shaped common contact section.

18. (Previously Presented) A semiconductor integrated circuit device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns,

wherein each of the nonvolatile semiconductor memory devices comprises:

a word gate formed on a semiconductor layer with a first gate insulating layer therebetween;

an impurity diffusion layer which forms either a source region or a drain region; and

first and second control gates in the shape of sidewalls formed along either side of the word gate, wherein:

the first control gate is disposed on the semiconductor layer with a second gate insulating layer therebetween, and also on the word gate with a side insulating layer therebetween;

the second control gate is disposed on the semiconductor layer with another second gate insulating layer therebetween, and also on the word gate with another side insulating layer therebetween;

the first and second control gates extend in a first direction; and

a pair of the first and second control gates, adjacent each other in a second direction which intersects the first direction, are connected to each other through a pad-shaped common contact section that is disposed in a staggered arrangement relative an adjacent common contact section, the pair of the first and second control gates also being connected to an upper interconnect layer through a conductive layer disposed in a contact hole and formed over the pad-shaped common contact section.

19. (Previously Presented) The semiconductor integrated circuit device of claim 18, wherein the common contact section includes an insulating layer formed on the semiconductor layer, the insulating layer formed of a laminate comprising a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.

20. (Previously Presented) The semiconductor integrated circuit device of claim 13,

wherein the common contact section is connected to the end of the first control gate and to the end of the second control gate, and includes a common contact section conductive layer that is formed of the same material as the first and second control gates.

21. (Currently Amended) A semiconductor integrated circuit device having a memory cell array in which nonvolatile semiconductor memory devices are arranged in a matrix with a plurality of rows and columns,

wherein each of the nonvolatile semiconductor memory devices comprises:

a word gate formed on a semiconductor layer with a first gate insulating layer therebetweeninterposed;

an impurity diffusion layer which forms either a source region or a drain region;

a first control gate in the shape of a sidewall formed along one side of the word gate and disposed on the semiconductor layer with a second gate insulating layer therebetweeninterposed, and also on the word gate with a side insulating layer therebetweeninterposed; and

a second control gate in the shape of a sidewall formed along another side of the word gate and disposed on the semiconductor layer with another second gate insulating layer therebetweeninterposed, and also on the word gate with another side insulating layer therebetweeninterposed,

wherein two nonvolatile semiconductor memory devices adjacent to each other in a row direction and share the impurity diffusion layer comprise: a pair of first and second control gates facing each other with the impurity diffusion layer therebetweeninterposed, are connected to each other surrounding the impurity diffusion layer and connected to a common contact section.

22. (Previously Presented) The semiconductor integrated circuit device as defined in claim 21,

wherein the common contact section is connected to the first and second control gates and includes a conductive layer formed of the same material as the first and second control gates.

23. (Previously Presented) The semiconductor integrated circuit device as defined in claim 21,

wherein the common contact section includes an insulating layer formed on the semiconductor layer, the conductive layer formed on the insulating layer, and a cap layer formed on the conductive layer.

24. (Previously Presented) The semiconductor integrated circuit device as defined in claim 23,

wherein the insulating layer is formed of a laminate consisting of a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.

25. (Previously Presented) The semiconductor integrated circuit device as defined in claim 21, wherein:

the side insulating layers are located between the word gate and the first and second control gates; and

the upper ends of the side insulating layers are located higher than the first and second control gates with respect to the semiconductor layer.

26. (Previously Presented) The semiconductor integrated circuit device as defined in claim 21, wherein:

a buried insulating layer is formed between the two side insulating layers disposed in contact with the first and second control gates; and

the buried insulating layer covers the adjacent first and second control gates.

27. (Previously Presented) The semiconductor integrated circuit device as defined in claim 21,

wherein the common contact section is provided in contact with one end of the impurity diffusion layer.

28. (Previously Presented) The semiconductor integrated circuit device as defined in claim 27,

wherein the common contact sections are staggered relative to each other.

29. (Previously Presented) The semiconductor integrated circuit device as defined in claim 21,

wherein the second gate insulating layer is formed of a laminate consisting of a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.

30. (Previously Presented) The semiconductor integrated circuit device as defined in claim 21,

wherein the side insulating layer is formed of a first silicon oxide layer, a silicon nitride layer, and a second silicon oxide layer.